

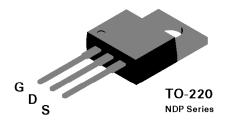
NDP7051 / NDB7051 N-Channel Enhancement Mode Field Effect Transistor

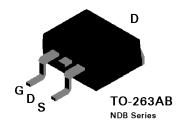
General Description

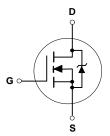
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 70A, 50V. $R_{DS(ON)} = 0.013\Omega$ @ $V_{GS} = 10V$.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7051	NDB7051	Units	
V _{DSS}	Drain-Source Voltage		V		
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 \text{ M}\Omega$)		V		
V _{GSS}	Gate-Source Voltage - Continuous	±	V		
	- Nonrepetitive (t _p < 50 μs)	±			
I _D	Drain Current - Continuous		А		
	- Pulsed	2			
P _D	Maximum Power Dissipation @ T _C = 25°C	•	130		
	Derate above 25°C	Derate above 25°C 0.87			
T _J ,T _{STG}	Operating and Storage Temperature Range	-65	°C		
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	2	275	℃	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, I_{D} = 70 \text{ A}$				500	mJ
I _{AR}	Maximum Drain-Source Avalanche Curre	nt				70	Α
OFF CH	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		50			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$				10	μΑ
			$T_{J} = 125^{\circ}C$			1	mA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	·			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAI	RACTERISTICS (Note 1)	·					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2	2.9	4	V
			T _J = 125°C	1.4	2.2	3.6	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 35 \text{ A}$	·		0.011	0.013	Ω
		T _J = 125°C			0.018	0.023	
I _{D(on)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		60			Α
g _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 35 \text{ A}$			30		S
DYNAMI	CCHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$			1930		pF
C _{oss}	Output Capacitance	f = 1.0 MHz			870		pF
C _{rss}	Reverse Transfer Capacitance		1				pF
SWITCHI	NG CHARACTERISTICS (Note 1)	-		•		·	
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 25 \text{ V}, I_{D} = 70 \text{ A},$			13	30	nS
t _r	Turn - On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 5 \Omega$			98	200	nS
t _{D(off)}	Turn - Off Delay Time			36	80	nS	
t _f	Turn - Off Fall Time				65	150	nS
Q _a	Total Gate Charge	$V_{DS} = 48 \text{ V},$			67	100	nC
Q_{gs}	Gate-Source Charge	$I_D = 70 \text{ A}, V_{GS} = 10 \text{ V}$			11		nC
Q_{gd}	Gate-Drain Charge				38		nC

Symbol	Parameter	Min	Тур	Max	Units	
DRAIN-S	OURCE DIODE CHARACTERISTICS	•				
S	Maximum Continuos Drain-Source Diode			70	А	
SM	Maximum Pulsed Drain-Source Diode For			210	Α	
/ _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 35 A (Note 1)		0.9	1.3	V
		T _J = 125°C		0.8	1.2	1
r	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = 70 \text{ A}, dI_F/dt = 100 \text{ A/}\mu\text{s}$	40	105	150	ns
r	Reverse Recovery Current		2	4.5	10	Α
HERMA	L CHARACTERISTICS	•				
R _B JC	Thermal Resistance, Junction-to-Case				1.15	°C/W
R _{OJA}	Thermal Resistance, Junction-to-Ambient			62.5	°C/W	

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

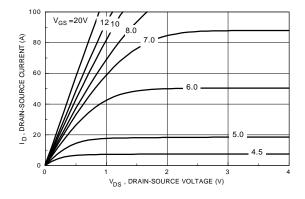


Figure 1. On-Region Characteristics.

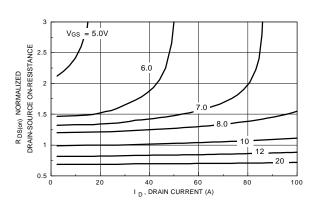


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

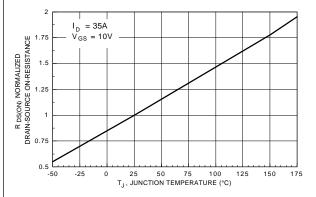


Figure 3. On-Resistance Variation with Temperature.

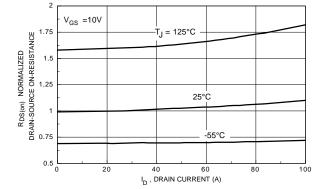


Figure 4. On-Resistance Variation with Drain Current and Temperature.

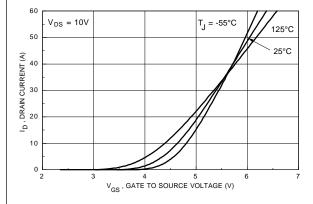


Figure 5. Transfer Characteristics.

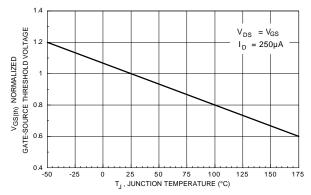


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

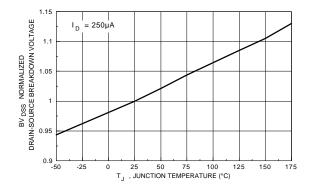


Figure 7. Breakdown Voltage Variation with Temperature.

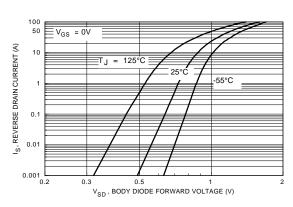


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

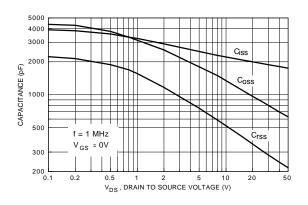


Figure 9. Capacitance Characteristics.

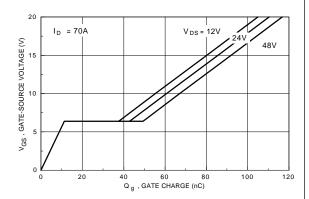


Figure 10. Gate Charge Characteristics.

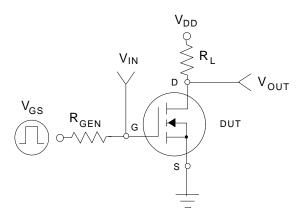


Figure 11. Switching Test Circuit.

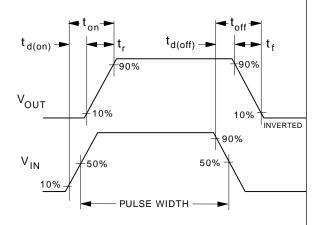
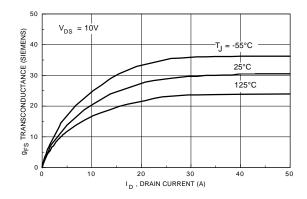


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



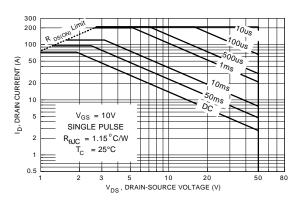


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

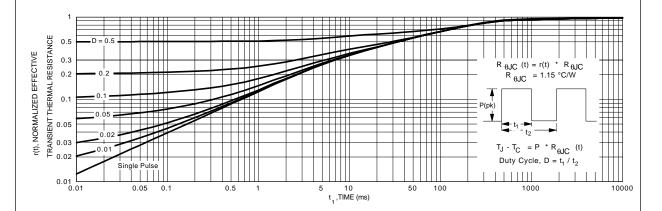
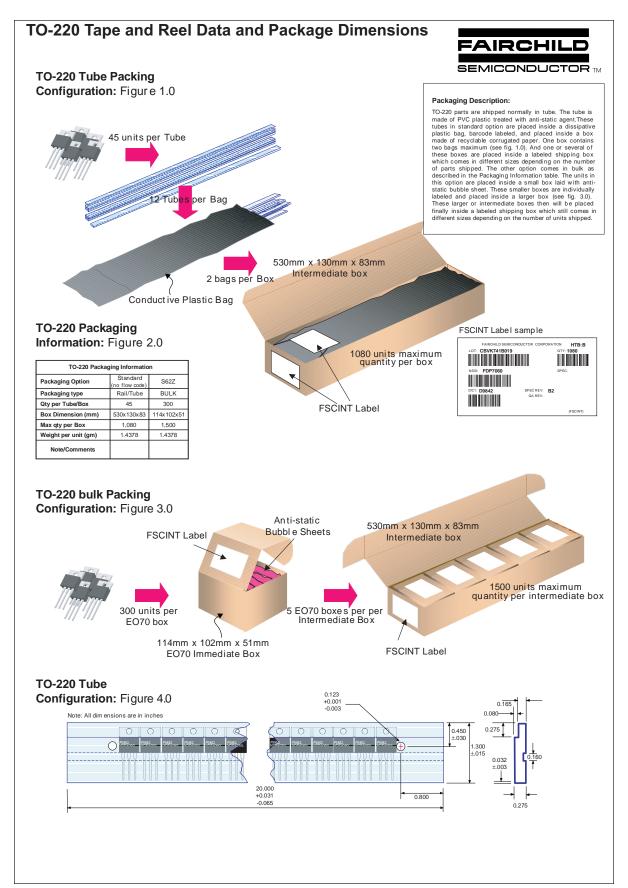
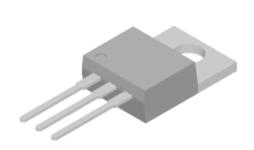


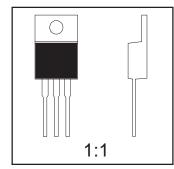
Figure 15. Transient Thermal Response Curve.



TO-220 Tape and Reel Data and Package Dimensions, continued

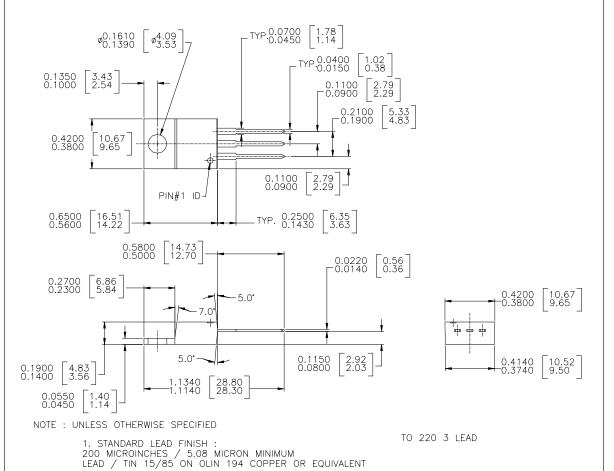
TO-220 (FS PKG Code 37)

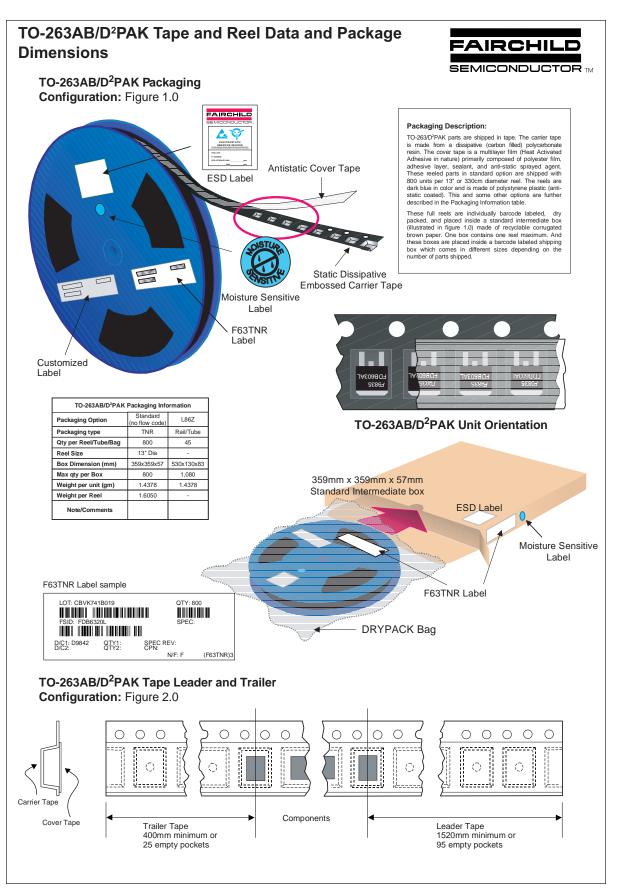




Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

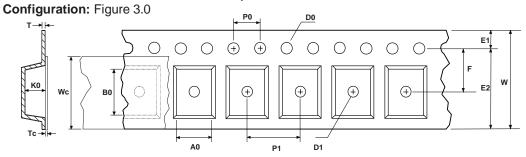
Part Weight per unit (gram): 1.4378





TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

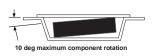
TO-263AB/D²PAK Embossed Carrier Tape



User Direction of Feed

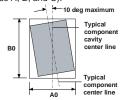
Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D ² PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)

Component Rotation

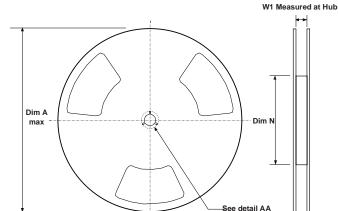


Sketch B (Top View)
Component Rotation

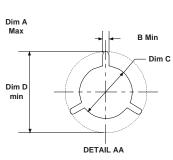


Sketch C (Top View)
Component lateral movement

TO-263AB/D²PAK Reel Configuration: Figure 4.0



13" Diameter Option



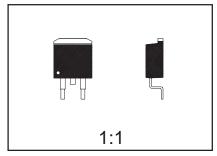
W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

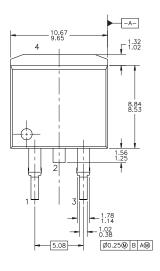
TO-263AB/D²PAK (FS PKG Code 45)

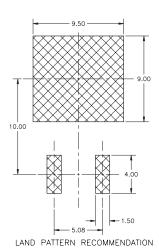


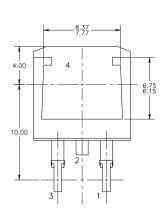


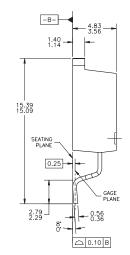
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) STANDARD LEAD FINISH:
 200 MICROINCHES / 5.08 MICROMETERS MIN.
 LEAD/TIN 15/85 ON OLIN 194 COPPER OR
 EQUIVALENT.
 C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
 TO EXCEED 0.003 INCH / 0.05mm.
 D) NO PACKAGE CHIPS, CRACKS OR SURFACE
 IDENTIFICATION ALLOWED AFTER FORMING.
 E) REFERENCE JEDEC, TO—265, ISSUE C,
 VARIATION AB, DATED 2/92.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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